

UMA (11.6")

Intel Brasswell-M Platform Block Diagram

+3VS5/+5VS5	PG.29
MOIC	PG.31
CPU Core	PG.32,33
DDR3L	PG.30
Charger	PG.28

DDR3L Memory down*4pcs	PG.14
DDR3L Memory down*4pcs	PG.15

1600MT/s
Channel A1600MT/s
Channel B

Intel Brasswell

Power : 4.5 (Watt)

Package : BGA1170

Size : 25 X 27 (mm)

eDP (2 lane)

EDP panel

PG.18

DP Port0

HDMI

PG.18

eMMC 4.51

eMMC
32G/64G

USB 3.0

USB 2.0

USB 2.0

USB 2.0

USB3.0 Ports
X1

PG.23

USB2.0 Ports
X1

PG.23

PCI-E x2

Card Reader
RTS5239-GR

PG.17

WLAN
BT COMBO
NGFF M2

PG.24

PG.2-13

WLAN
BT COMBO
NGFF M2

PG.24

Webcam

PG.18

WWAN
NGFF M2

PG.20

KBC
IT8987

PG.25

LPC

Fast SPI

KB

PG.21

TP

PG.21

ROM

PG.5

Azalia

AUDIO
CODEC
ALC 3227

PG.19

Speaker

PG.19

Without amp for eMMC sku

Headphone
amplifier

HPA022642RTJR

Daughter board

Hp

MIC

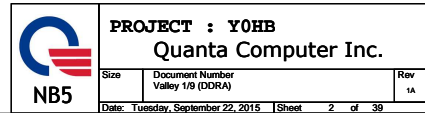
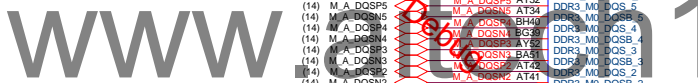
Combo Jack

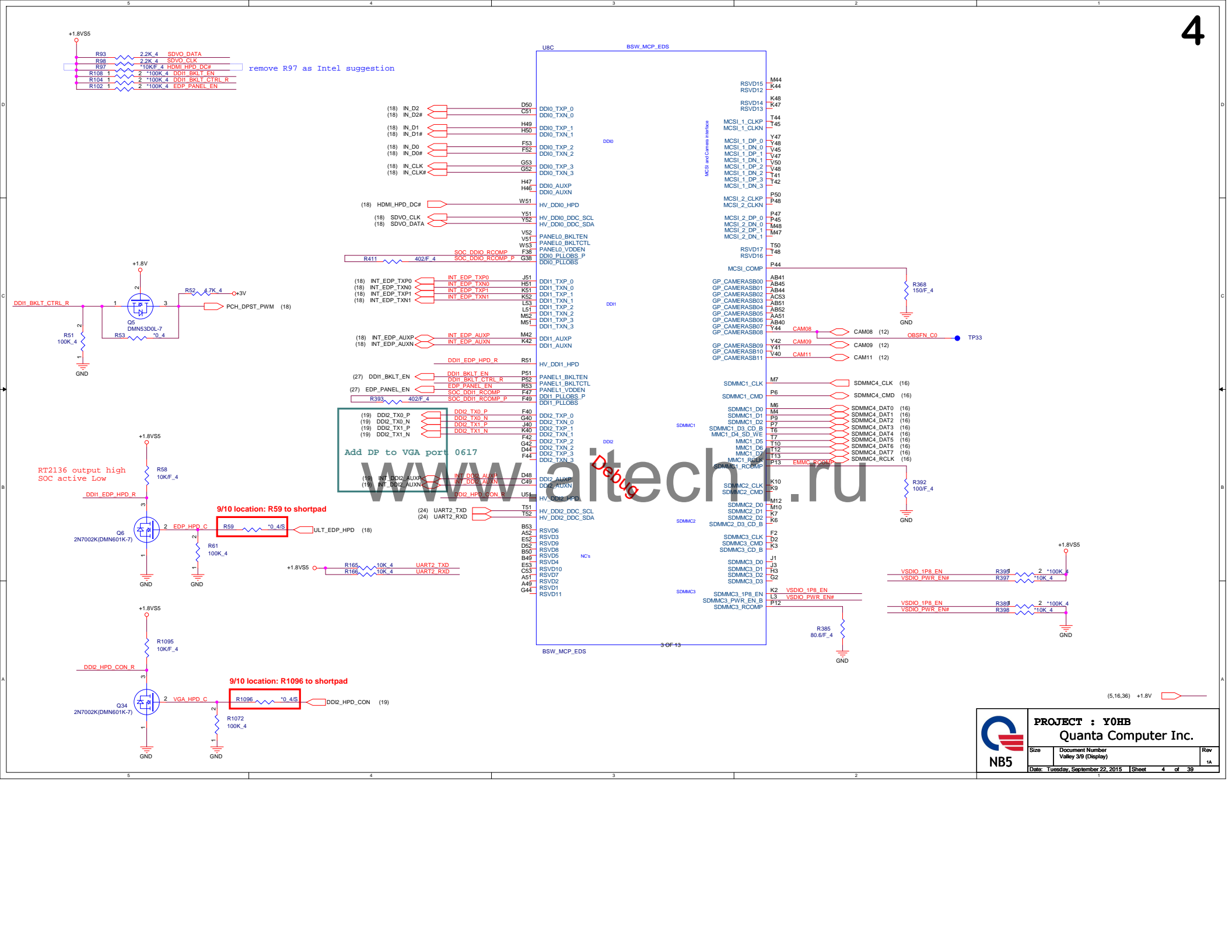
Daughter board



PROJECT : Y0HB
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	1A
Date:	Tuesday, September 22, 2015	Sheet 1 of 39




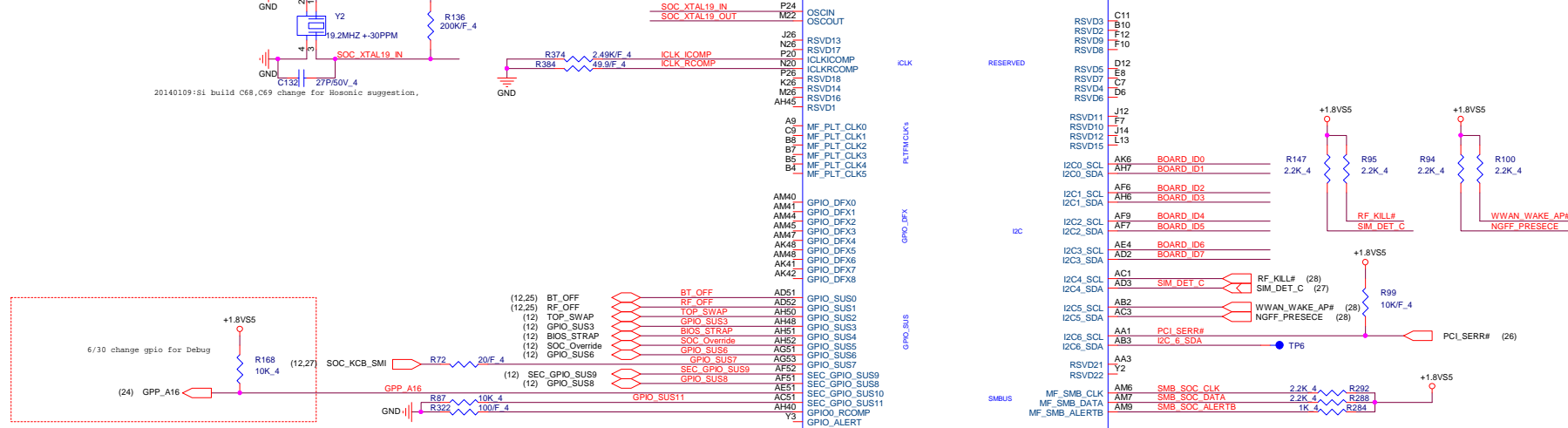




Vender	Size	P/N
Winbond	8MB	AKE5EZNN0N1 (W25Q64FWSSIQ)
GigaDevice	8MB	AKE5EG-0Q00 (GD25LQ64CSIGR)
	8MB	AKE5EFN0Q00 (EN25S64-104HIP)
Socket (208mil)		DFHS08FS023 (Firstly Stuff)



	PROJECT : Y0HB Quanta Computer Inc.		
	Size	Document Number Valley 4/9 (SD/PCIE/SATA)	Rev 1A
Date: Tuesday, September 22, 2015		Sheet 5 of 39	

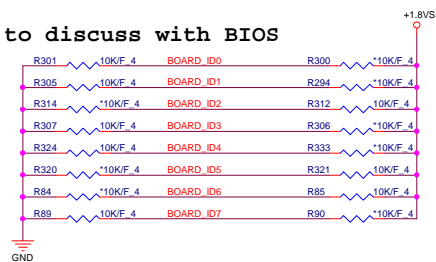


www.aitech1.ru

BOARD ID SETTING

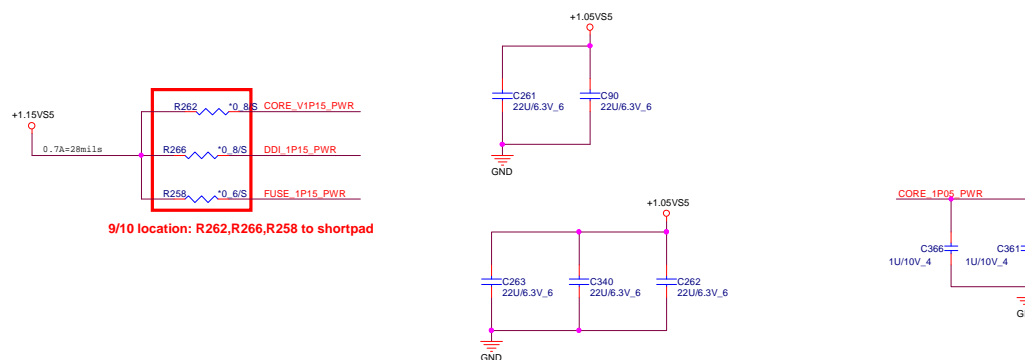
	Reserve (Default = 000)			Size	TPM	Storage		Reserved
Model	BOARD_ID7	BOARD_ID6	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID0	BOARD_ID1	BOARD_ID2
Samsung(Q)	0	1	0	2G=0	0 : N/A	0	0	0 : emmc
Mircon	0	0	1	4G=1	1 : TPM	0	0	1 : HDD
Hynix	0	0	0			0	0	
Samsung(E)	0	1	1			0	0	

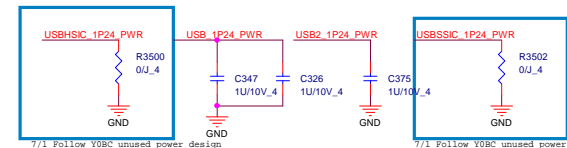
Need to discuss with BIOS





Size	Document Number Valley 6/9 (USB/LPC/12C)	Rev
Date:	Tuesday, September 22, 2015	Sheet 8 of 39

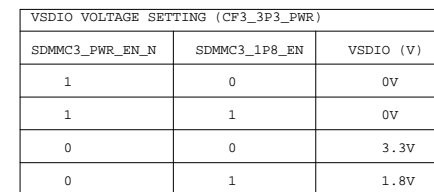


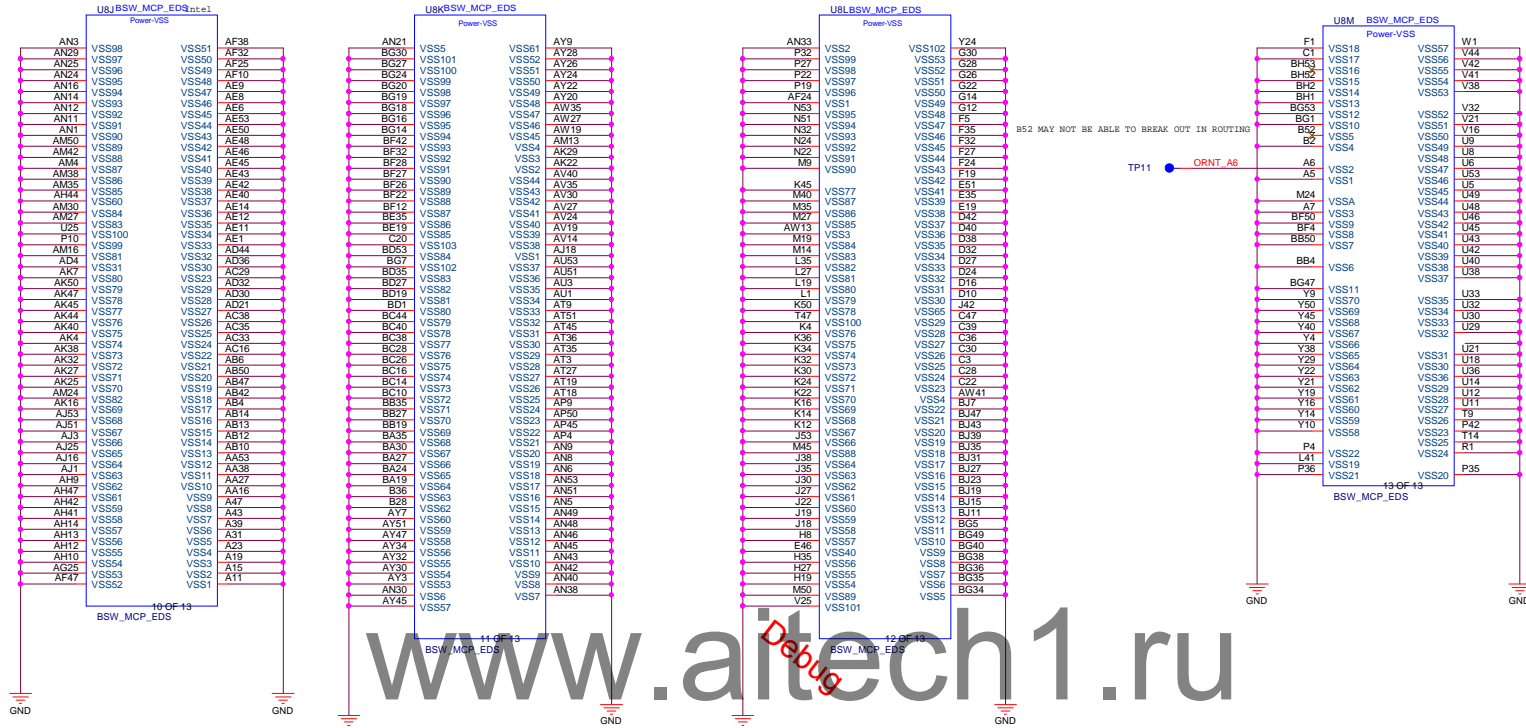


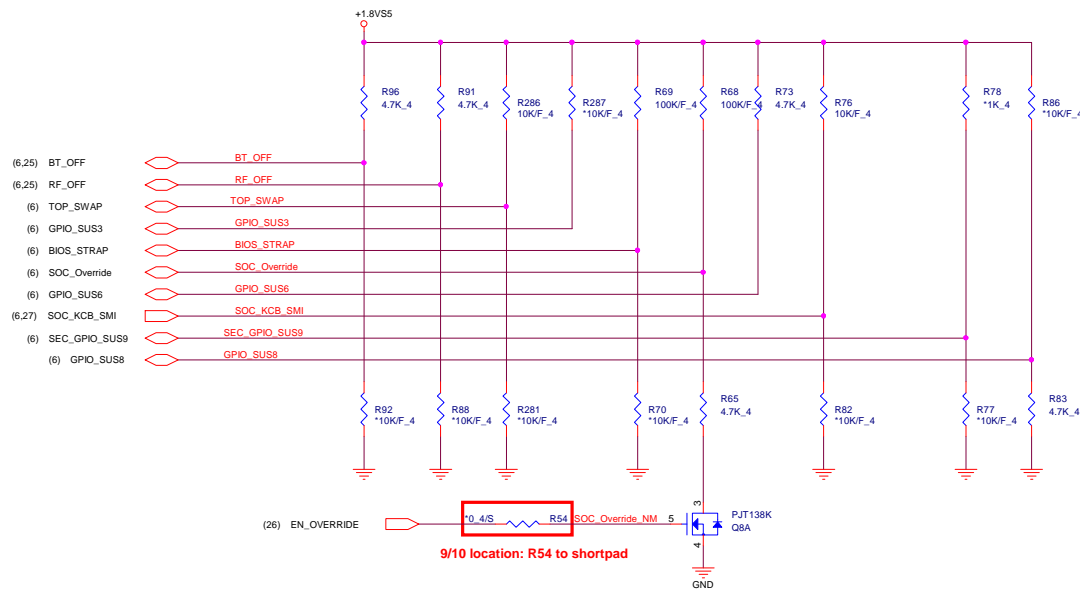
7/1 Follow Y0BC unused power design

7/1 Follow Y0BC unused power design

9/10 location: R433,R351,R413,R359,R338,R405 to shortpad



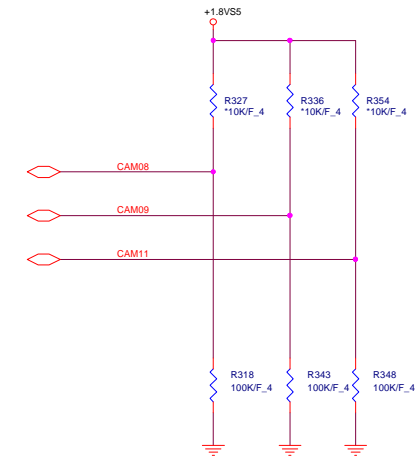




(4) CAM08

(4) CAM09

(4) CAM11



REQUIRED STRAPS

	GPIO_SUS0	GPIO_SUS1	TOP_SWAP	GPIO_SUS3	BIOS_STRAP	SOC_Override	GPIO_SUS6	SOC_KCB_SMI	GPIO_SUS8
PULL HIGH	DDI0 detected DEFAULT	DDI1 detected DEFAULT	Normal Operation DEFAULT	Reserve 10 KΩ PU DEFAULT	SPI DEFAULT	Normal Operation DEFAULT	10 KΩ PU to 1.8V DEFAULT	Reserve 10 KΩ PU DEFAULT	Supply is 1.35V DEFAULT
PULL LOW	DDI0 not detected	DDI1 not detected	Change Boot Loader address		LPC	Override DEFAULT			Supply is 1.25V DEFAULT

	CAM08	CAM09	CAM11
PULL HIGH	ICLK Xtal OSC Bypass	CCU SUS RO Bypass	RTC OSC Bypass
PULL LOW	ICLK Xtal OSC No Bypass DEFAULT	CCU SUS RO No Bypass DEFAULT	RTC OSC No Bypass DEFAULT

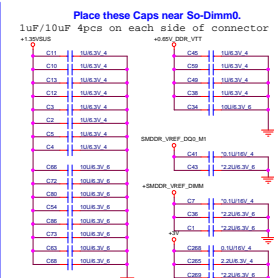


PROJECT : Y0HB
Quanta Computer Inc.

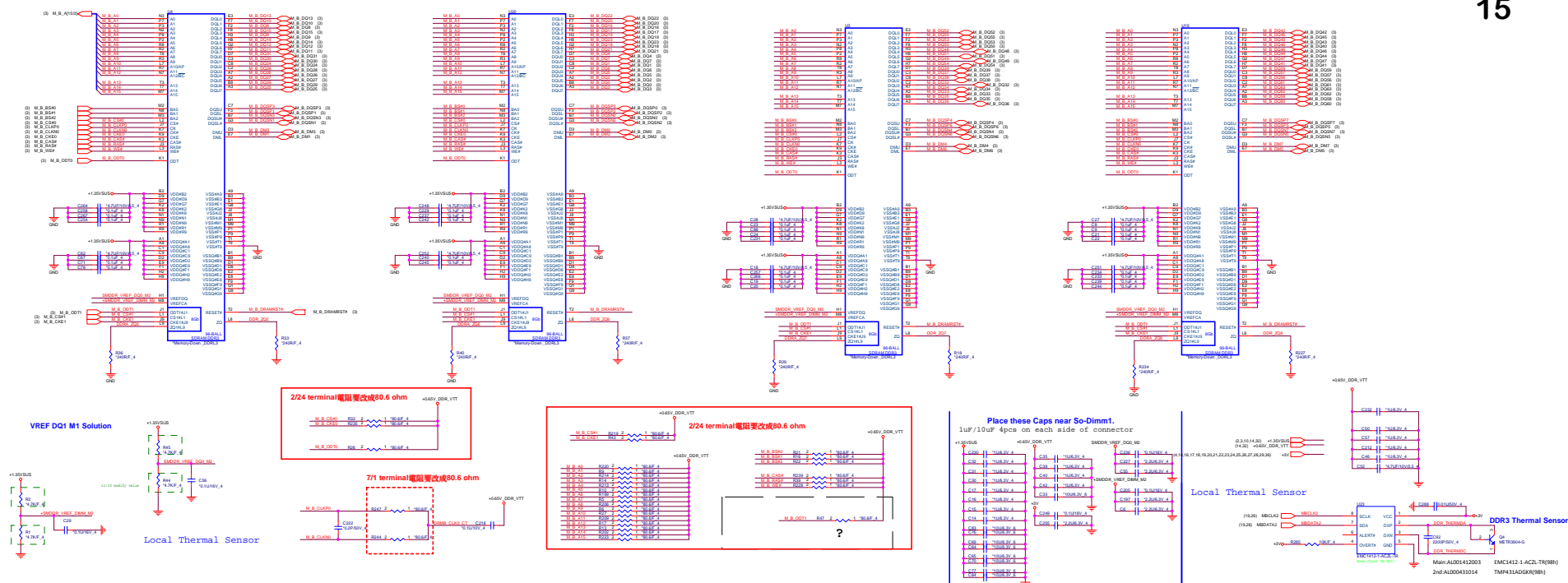
Size	Document Number	Rev
	Valley 9/9 (GND)	1A

Date: Tuesday, September 22, 2015 | Sheet 12 of 39

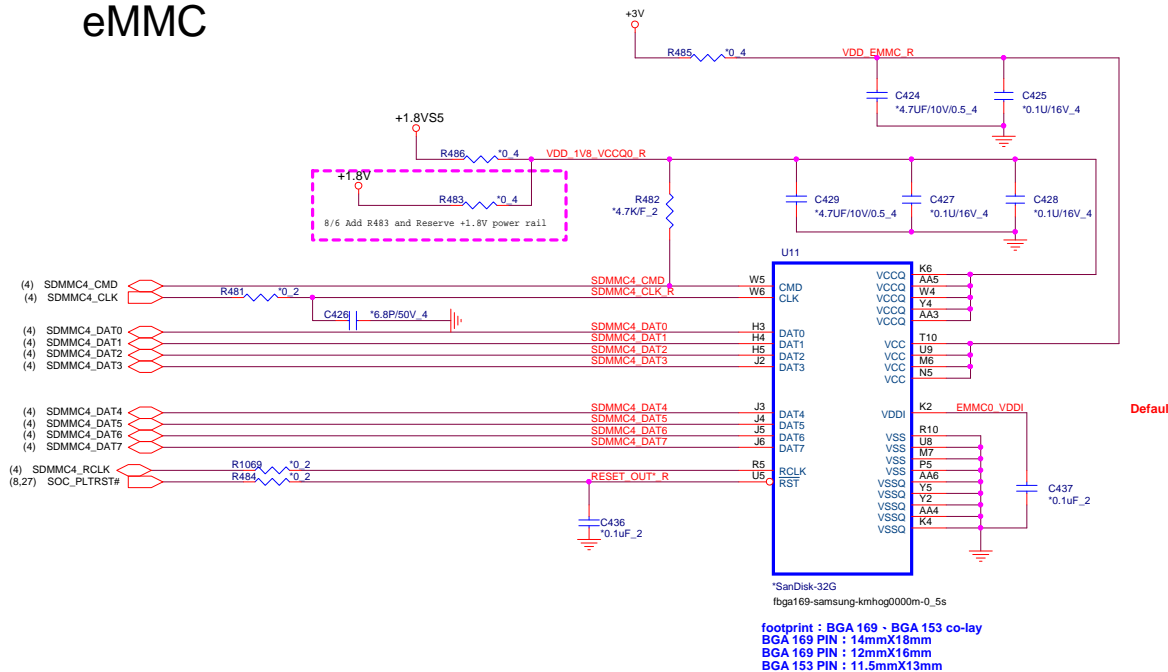
www.aitech1.ru



TPPS PN	QCCN	Vendor PN	Location	
AKDPSG1508	AKDPSJ0ETW18	H5T4C666R-F-PBA	IC SRAM (6P) H5T4C666R-F-PBA	Hynix (Default)
AKDPSG1508	AKDPSG1509	K4B4G1646G-HYK10	IC SRAM (6P) K4B4G1646G-HYK10	Samsung U
AKDPSG1518	AKDPSG1519	MT41K256M1L-107-N	IC DRAM (6P) MT41K256M1L-107-N	Micron
AKDPSG1W14	AKDPSG1W15	H5T4C666R-F-PBA	IC SRAM (6P) H5T4C666R-F-PBA	Hynix (New ID)
AKDPSG1503	AKDJSJ00T502	K4B4G1646G-BYK10	IC SRAM (6P) K4B4G1646G-BYK10	Samsung E



www.aitech1.ru



Default

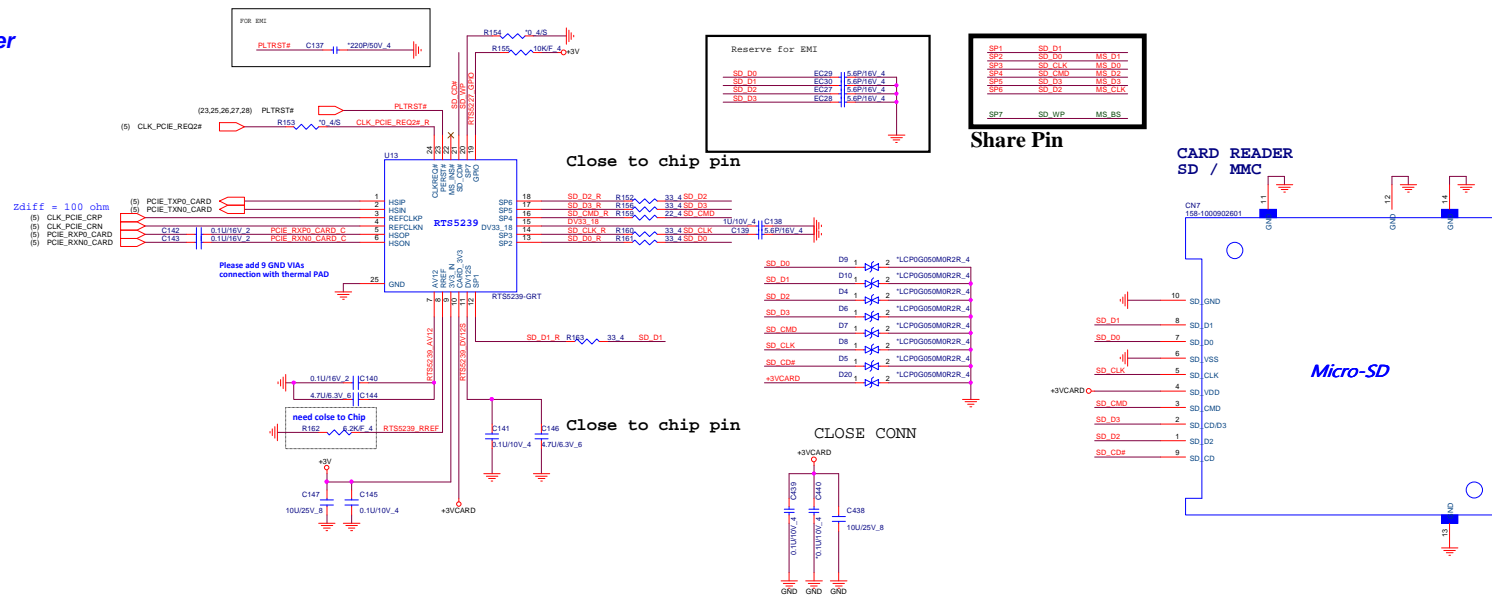
INAND (eMMC) V4.51				
TOPBSQ	QBCON	Description	SIZE	Vender
AKE3SZ-TW01	AKE3SZ-TW02	IC FLASH(153P)H26M64103EMR(FBGA)	32G	Hynix
	AKE5SZ0T512	IC FLASH(153)KLMBG4GEND-B031(FBGA)	32G	samaung
AKE3SFUT000	AKE3SFUT001	IC FLASH(153P)SDIN9DW4-32G(FBGA)	32G	SanDisk
AKE3TG-TW01	AKE3TG-TW02	IC FLASH(153P)H26M78103CCR(FBGA)	64G	Hynix
	AKE3TZPT520	IC FLASH(153)KLMCG8GEND-B031(FBGA)	64G	samaung
AKE3TFUT101	AKE3TFUT102	IC FLASH(153P)SDIN9DW4-64G(FBGA)	64G	SanDisk

eMMC setting		Location				
Vender	SIZE	R526	R528	R527	R529	R530
Hynix	32G	1	0	0	0	0
samaung	32G	1	1	0	0	0
SanDisk	32G	1	1	1	0	0
Hynix	64G	1	1	1	1	0
samaung	64G	0	1	1	1	1
SanDisk	64G	0	0	1	1	1
Hynix	128G	0	0	0	1	1
samaung	128G	0	0	0	0	1
SanDisk	128G	0	0	0	0	0
		1	1	1	1	1

Memory setting		Location				
Vender	SIZE	R521	R522	R523	R524	R525
Hynix	2G	1	0	0	0	0
samaung	2G	1	1	0	0	0
Micron	2G	1	1	1	0	0
Hynix	4G	1	1	1	1	0
samaung	4G	0	1	1	1	1
Micron	4G	0	0	1	1	1
		0	0	0	1	1
		0	0	0	0	1
		0	0	0	0	0
		1	1	1	1	1

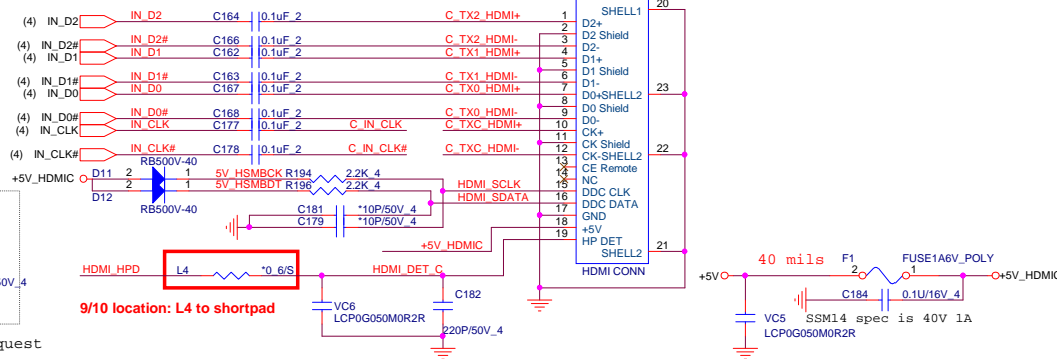
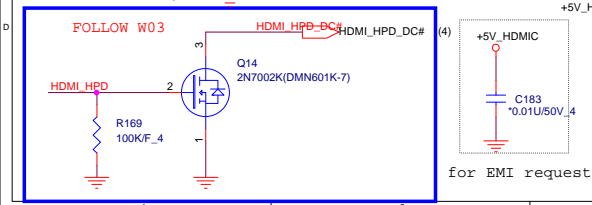
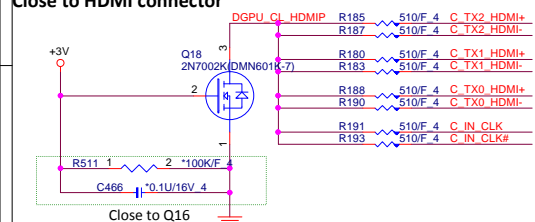
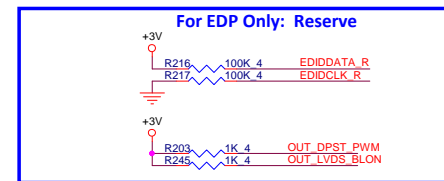
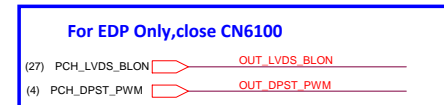
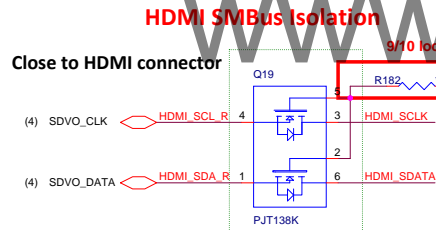
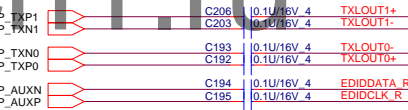
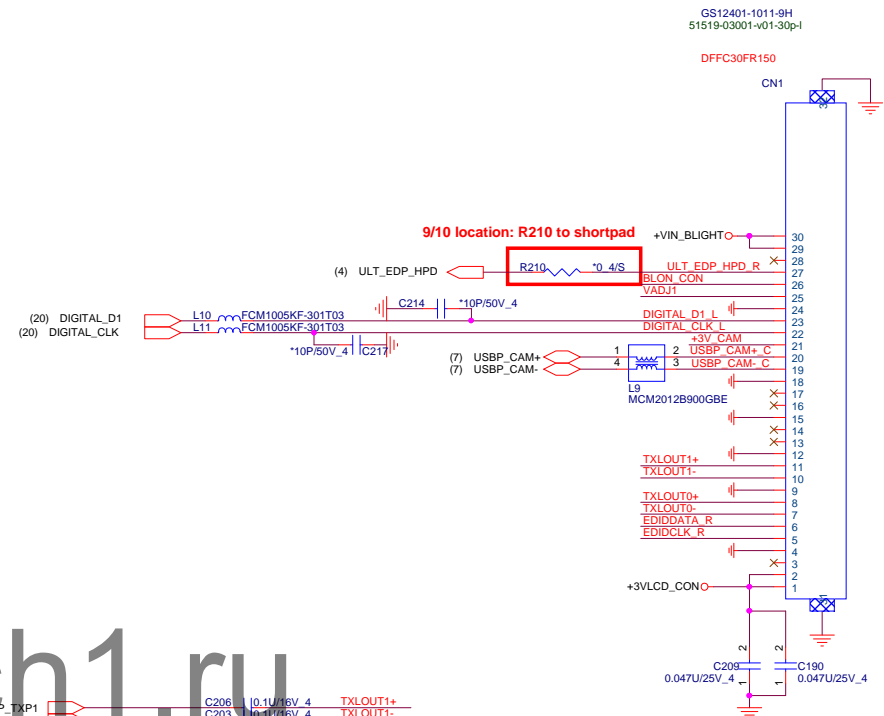
NB5	PROJECT : Y0HB		
	Quanta Computer Inc.		
Size	Document Number	TOPAZ S3 PCIE/DP power	1/4 Rev
Tuesday, September 22, 2015	Sheet	16of	39

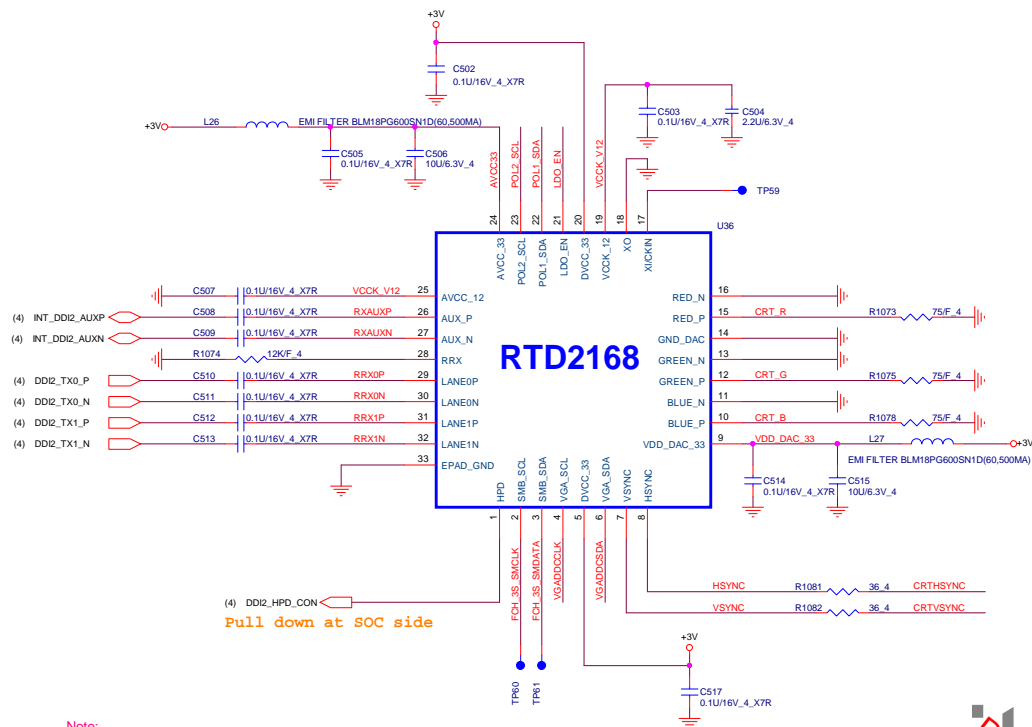
CardReader



www.aitech1.ru

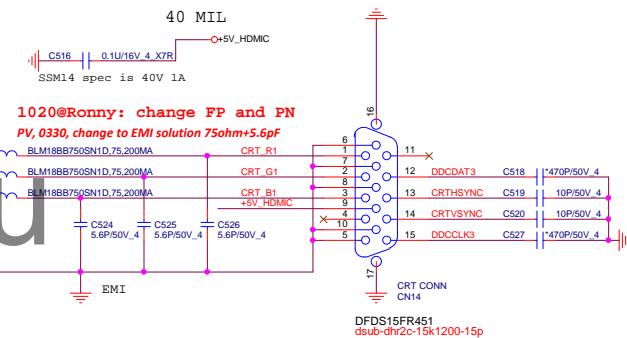
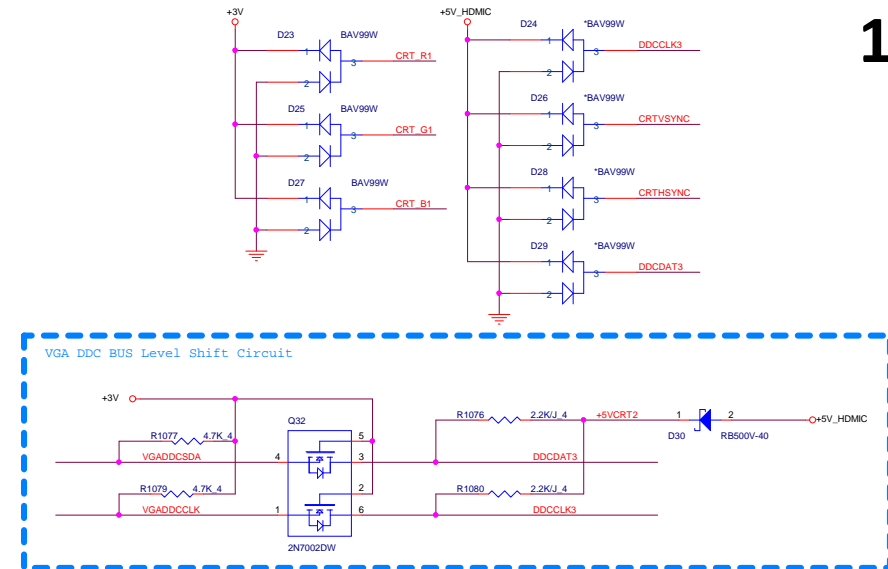
LVDS Conn. 18





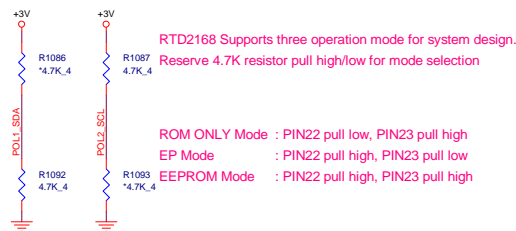
Note:

- 1- C1,C3,C6,C8,C9,C11,C12,C19,C20
Should be close to chip
- 2- C12 should be X5R material
- 3- R1 should be 12K ohm with +/-1%
- 4- R8, R9, R10 should be 75 ohm with +/-1%



Mode Configure Table(Power On Latch)

		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE



EEPROM MODE

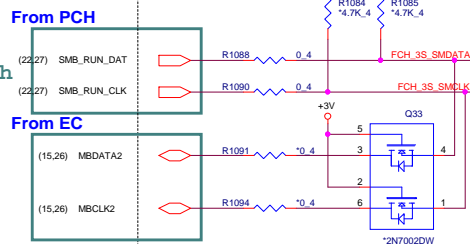
In EEPROM mode,an additional EEPROM is needed.
EEPROM should configure with following conditions.

- 1- EEPROM with a size of 16K-Byte
- 2- EEPROM device should be 2-byte addressing device
- 3- Slave address should configure as 0xA8

CIIC_SCL, CIIC_SDA Connection

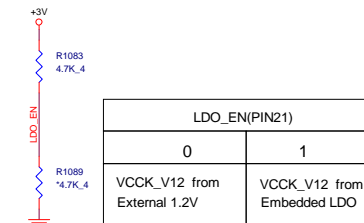
EP mode: Pin2, Pin3 connect to EC SMBUS
ROM or EEPROM mode: connect to PCH SMBUS
IIC Protocol is used

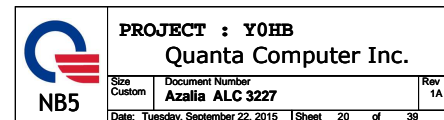
RTD2168 Slave Address:
0x64/0x65 and 0x68/0x69

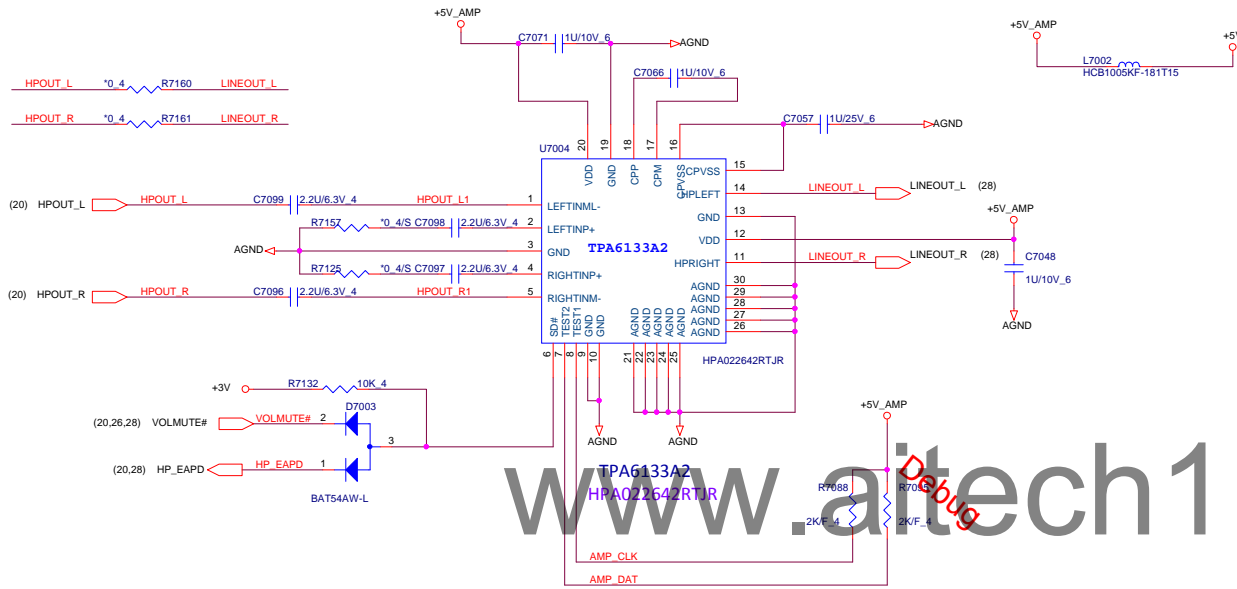


Embedded LDO

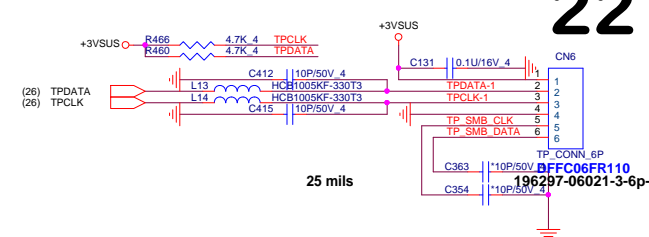
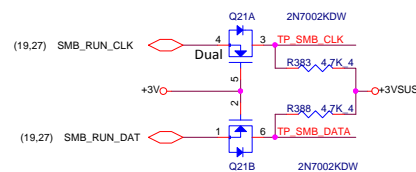
Select VCCK_V12 source from external 1.2V or embedded LDO





Head Phone out

www.aitech1.ru



(26) MY[0..15] MY0..15]

(26) MX[0..7] MX0..7]

MUTE_LED_CNTL_R1

Q31
2N7002K(DMM601K-7)

R520
10K/F_4

2

1

ED

R373 2 1 200F_6

R370 2 1 200F_6

200V CAPSLED5 R

1MUTE_LED_CNTL_R

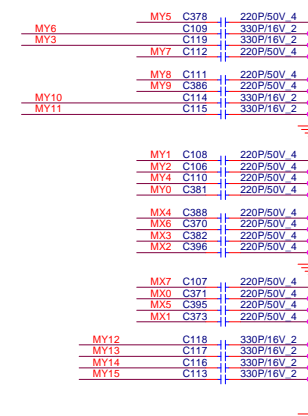
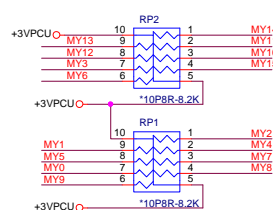
EC42
*0.1uF_4

KB1

30

29

KB_CONN_28P



www.aitech1.ru

Debug

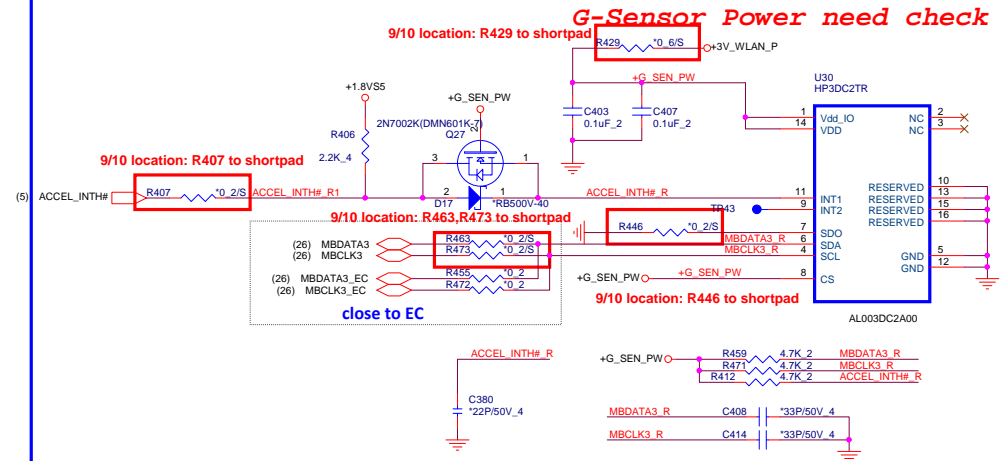
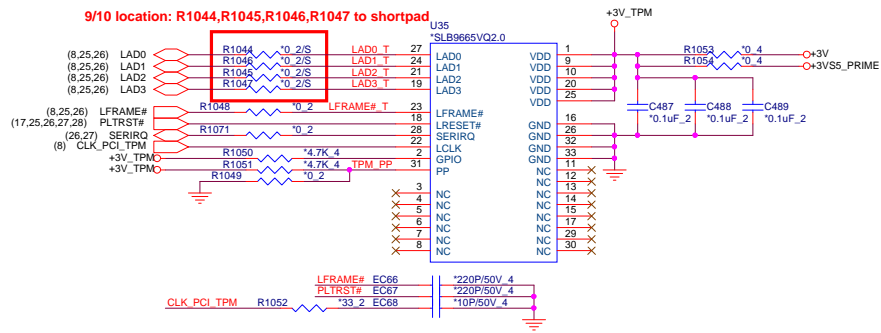
(4,14,15,16,17,18,19,20,21,23,24,25,26,27,28,29,36) +3V
 (18,20,21,24,28,29,36) +5V
 (8,10,24,25,26,27,28,30,31) +3VPCU



PROJECT : Y0HB
Quanta Computer Inc.

Size	Document Number TPM/TP/FAN/LED	Rev
Date: Tuesday, September 22, 2015	Sheet	22 of 39

Accelerometer Sensor

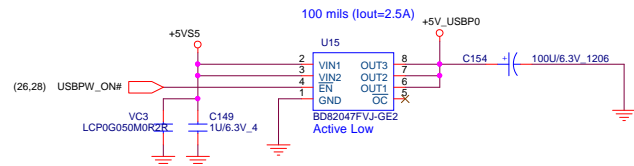


Touch screen

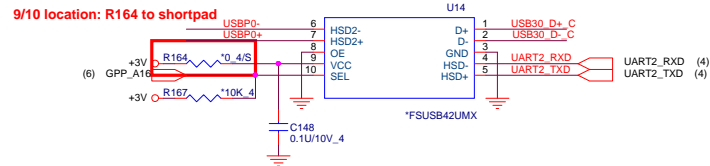
Green CLK Circuitry

www.aitech1.ru

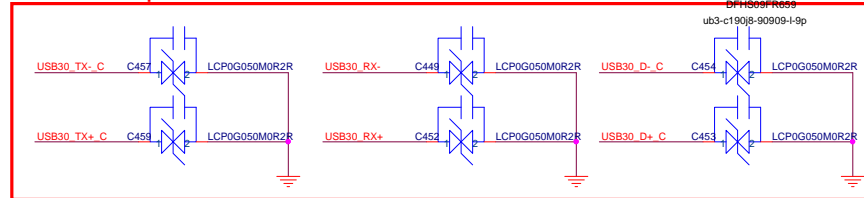
USB 2.0/3.0 Combo



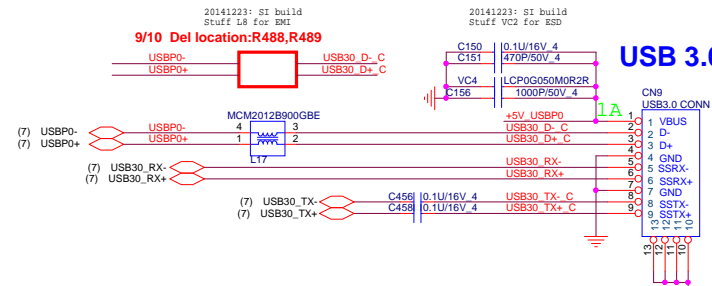
UART for DEBUG



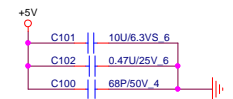
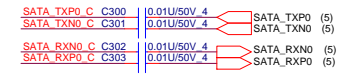
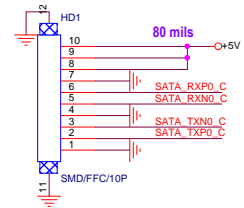
2/25 Add ESD part



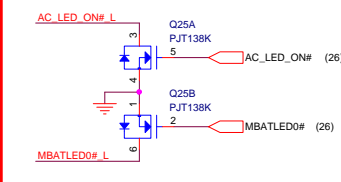
USB 3.0

**HDD**

3/24 Change pin define as Napa

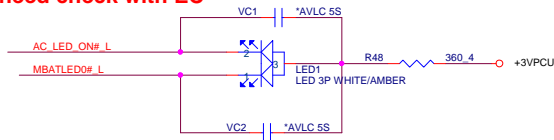


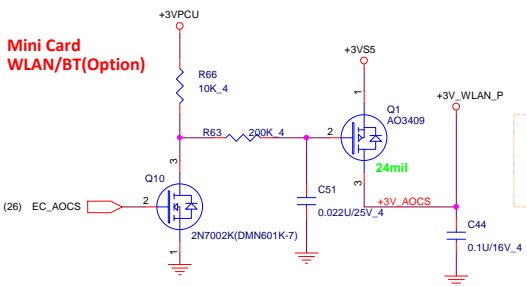
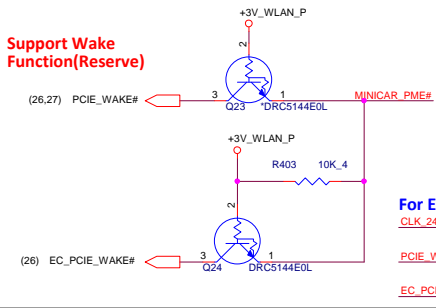
2/26 add LED MOS



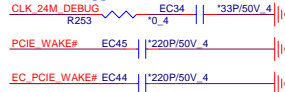
PWR LED

2/10 need check with EC



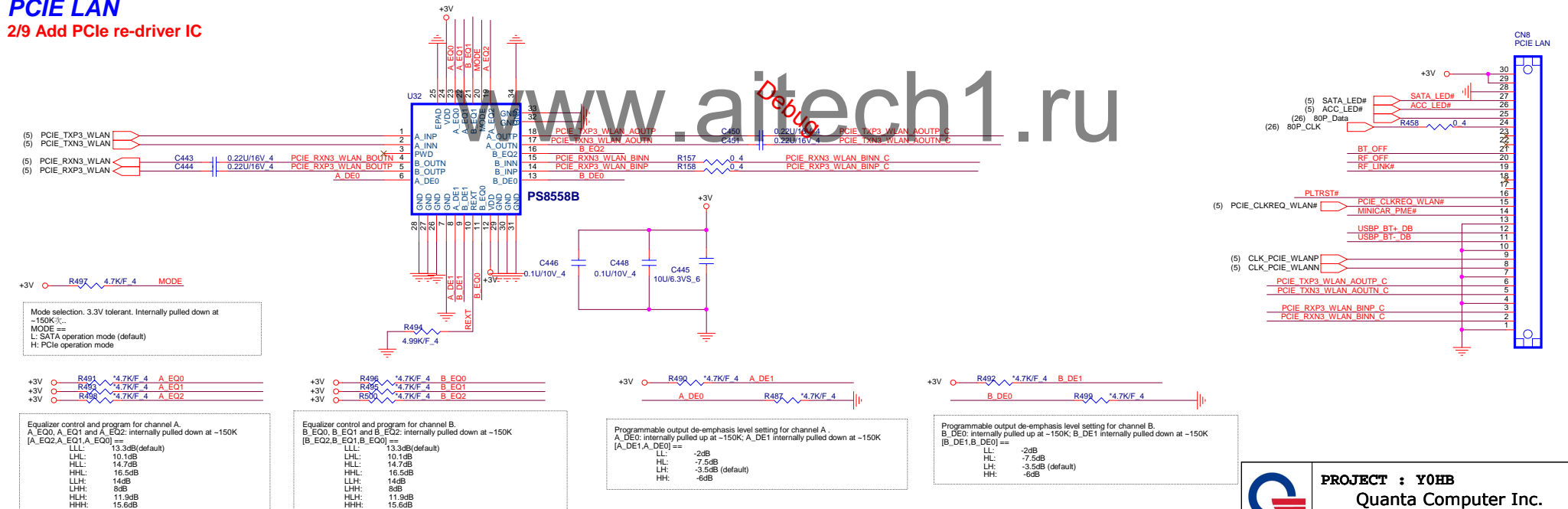
Mini Card
WLAN/BT(Optional)Support Wake
Function(Reserve)

For EMI Suggestion



PCIE LAN

2/9 Add PCIE re-driver IC

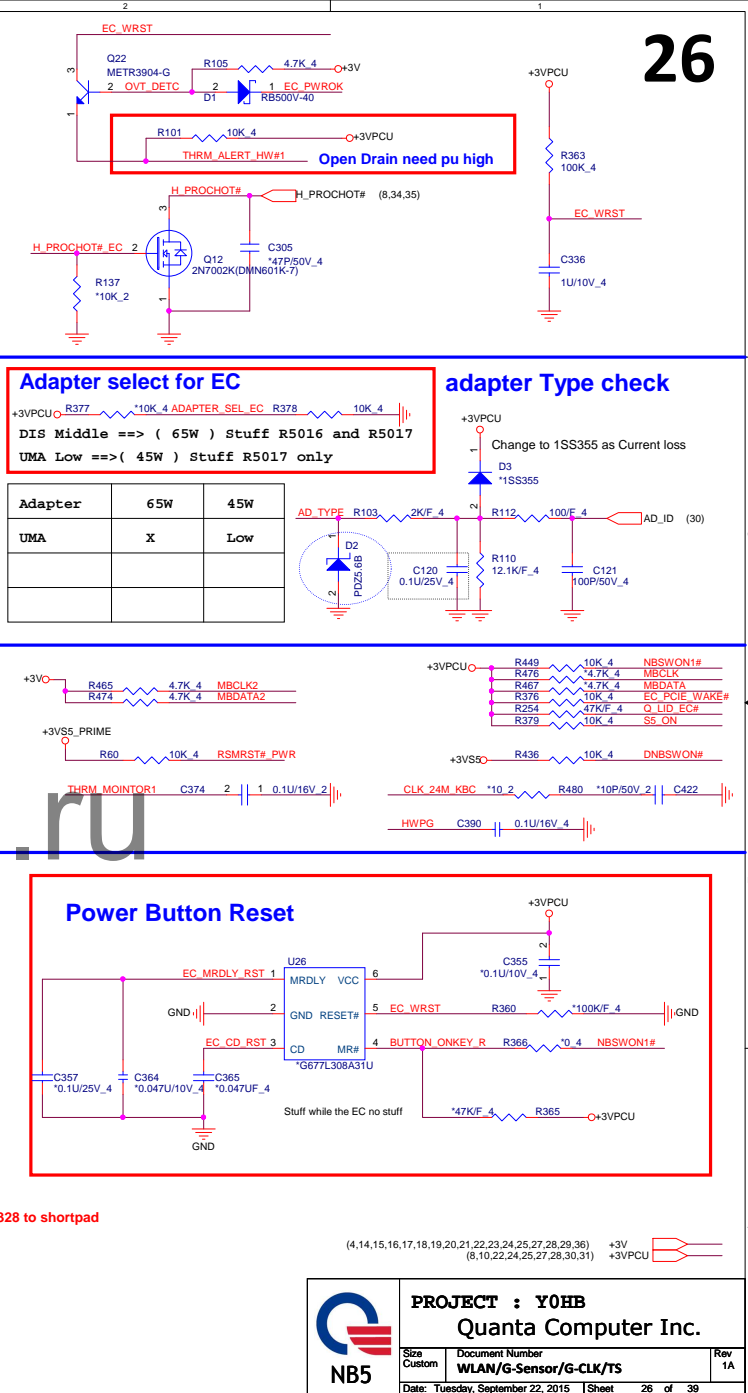
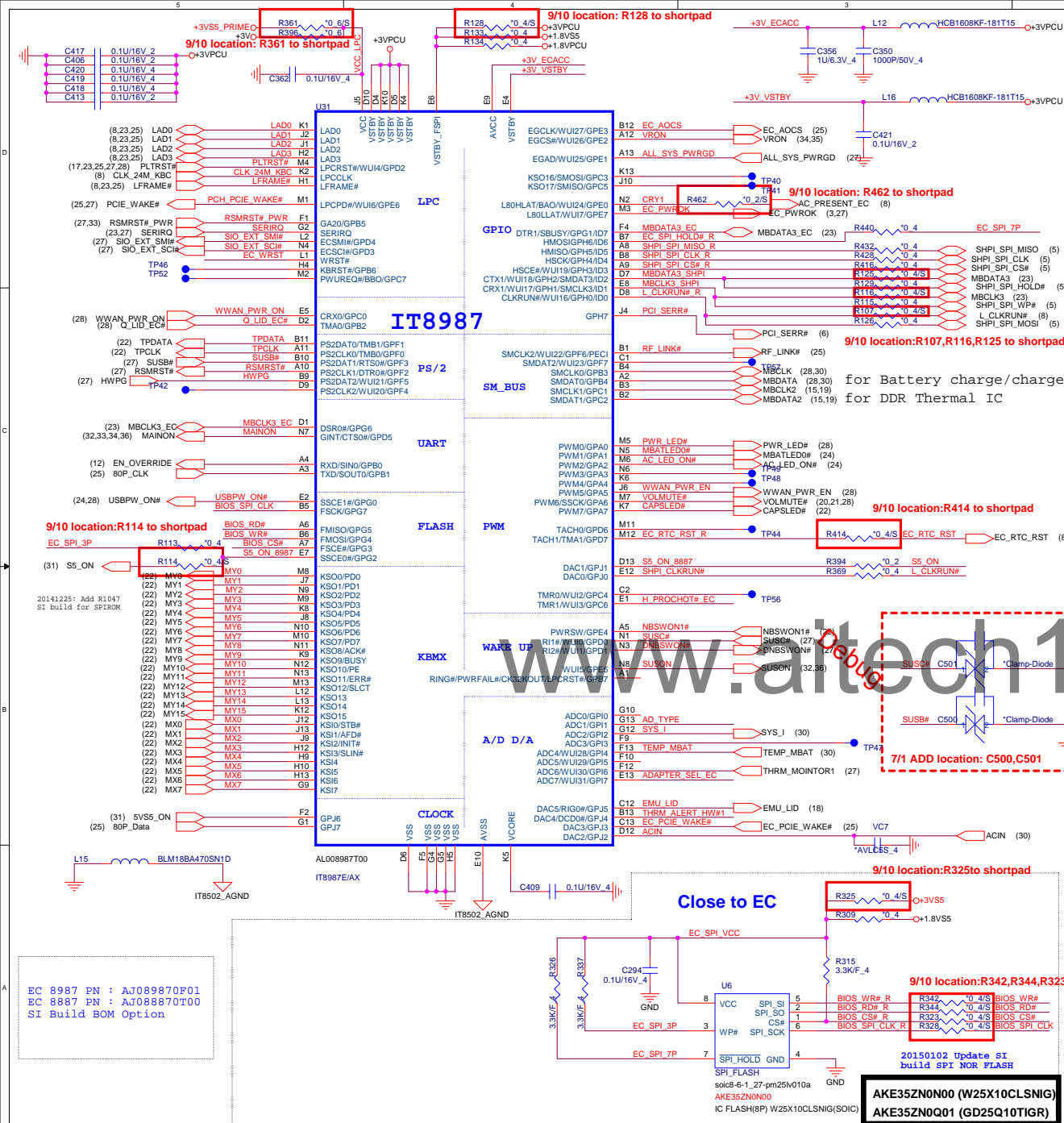


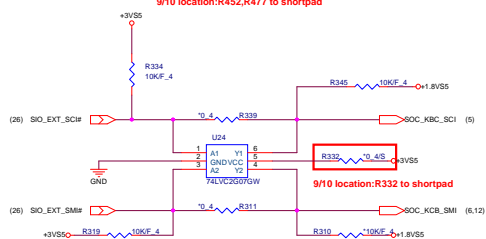
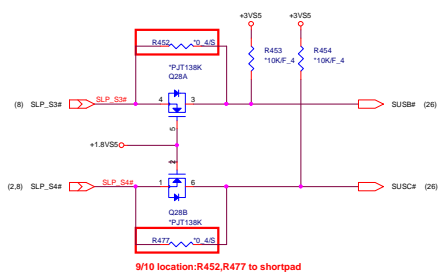
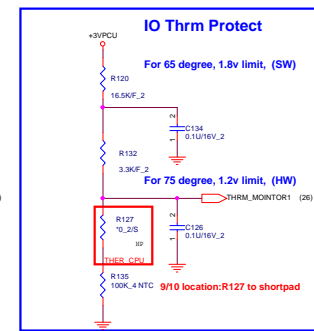
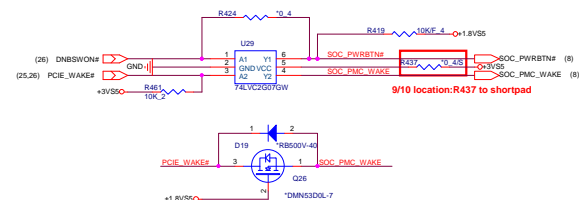
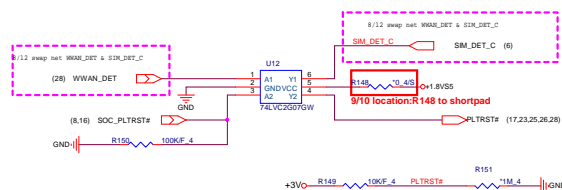
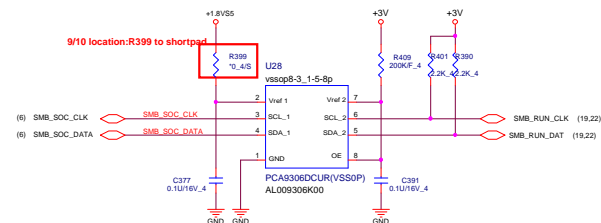
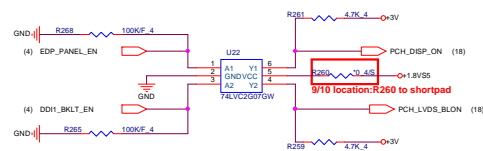
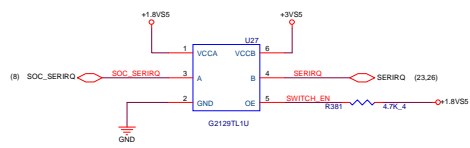
Chip power down. 3.3V tolerant. Internally pulled down at ~150K.
PWD ==
L: Normal operation (default)
H: Chip power down.



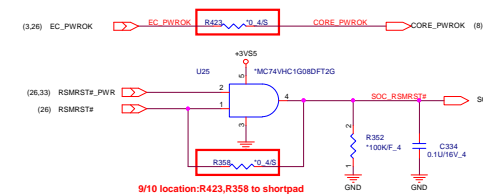
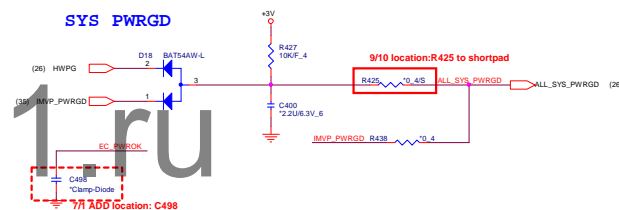
PROJECT : Y0HB
Quanta Computer Inc.

Size	Document Number	Rev
WLAN	WLAN	1A
Date: Tuesday, September 22, 2015	Sheet	25 of 39

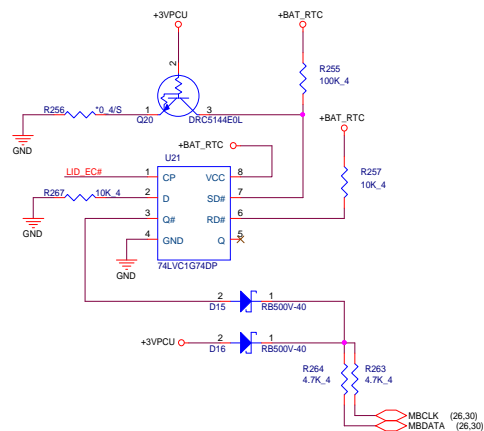




SYS PWRGD



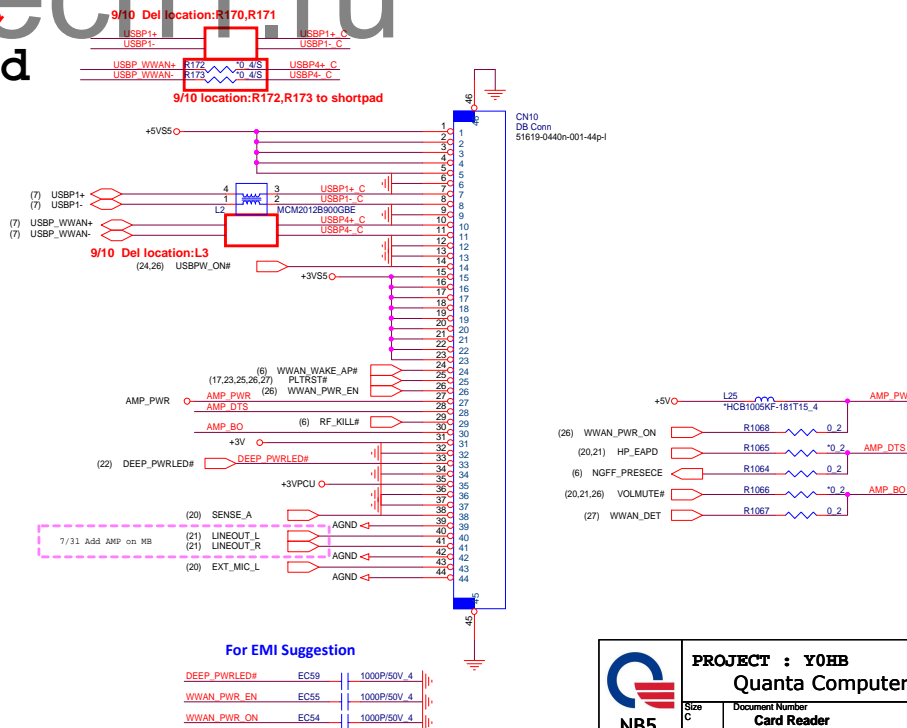
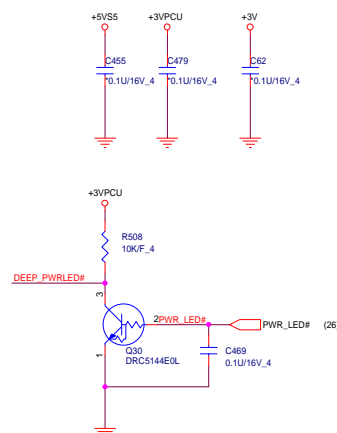
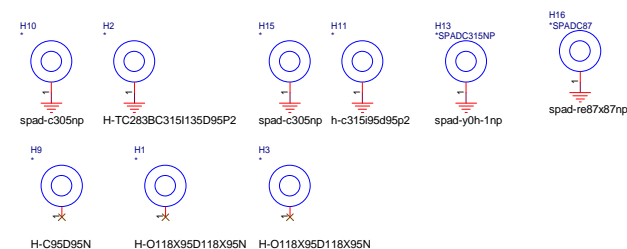
www.aitech1.ru



[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

[1] H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH CP transition;
 Q_{n+1} = state after the next LOW-to-HIGH CP transition.

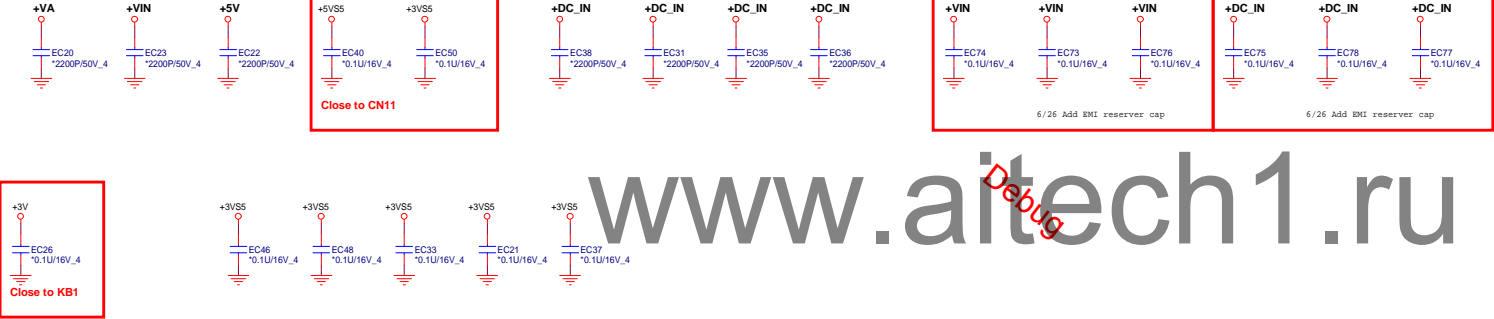
Thermal Nut



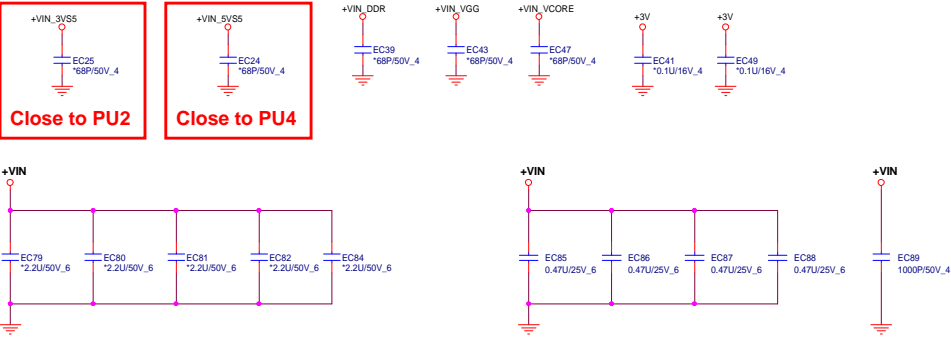
I/O port definition

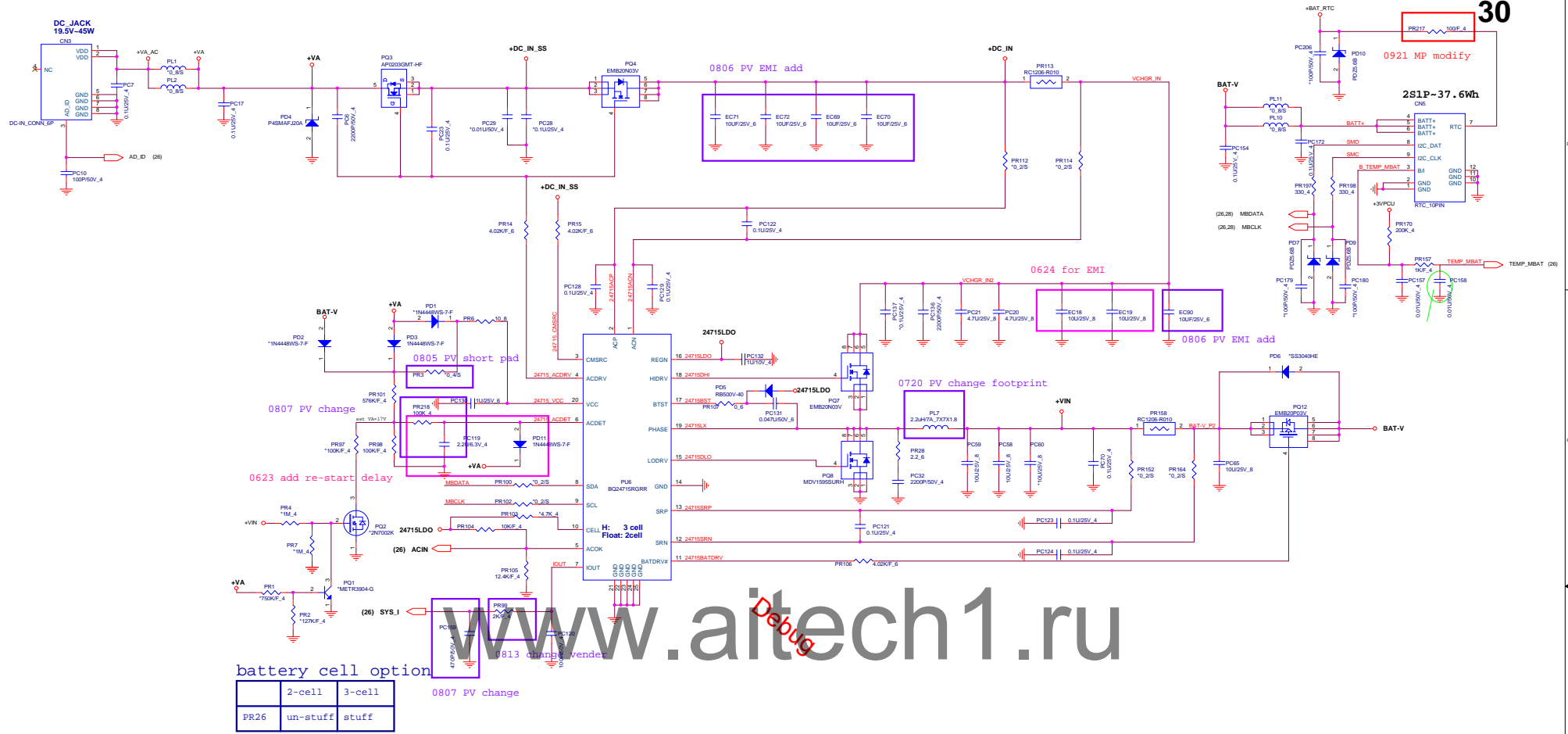
	Brasswell-M	Note
SATA Port0	HDD	
SATA Port1	ODD	
PCIE Port0	Card reader	
PCIE Port1		
PCIE Port2		
PCIE Port3	WIFI	
USB3.0 Port0	USB 2.0/3.0 Combo	
USB3.0 Port1		
USB3.0 Port2		
USB3.0 Port3		
USB2.0 Port0	USB 2.0/3.0 Combo	
USB2.0 Port1	USB 2.0	
USB2.0 Port2	Webcam	
USB2.0 Port3	BT	
USB2.0 Port4	WWAN	

EMI Reserve

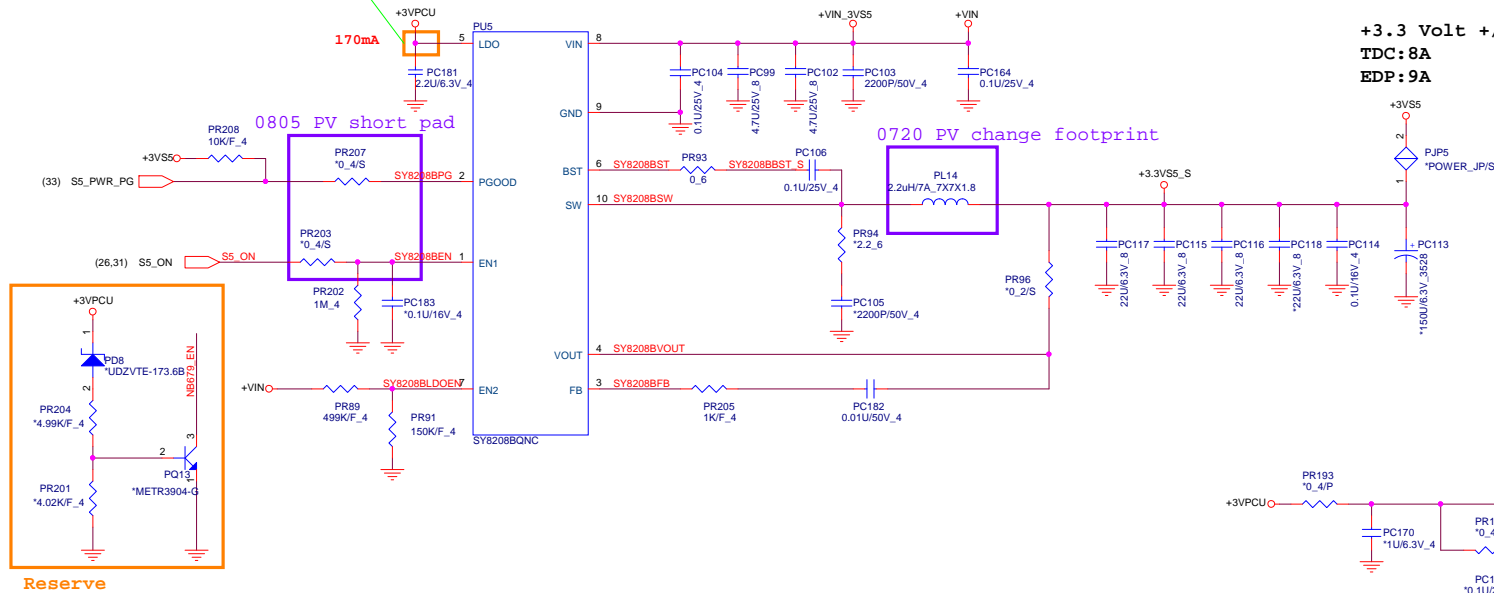


RF Reserve

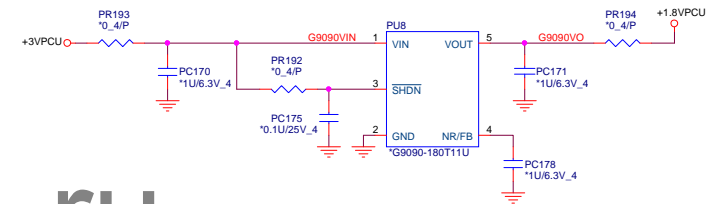




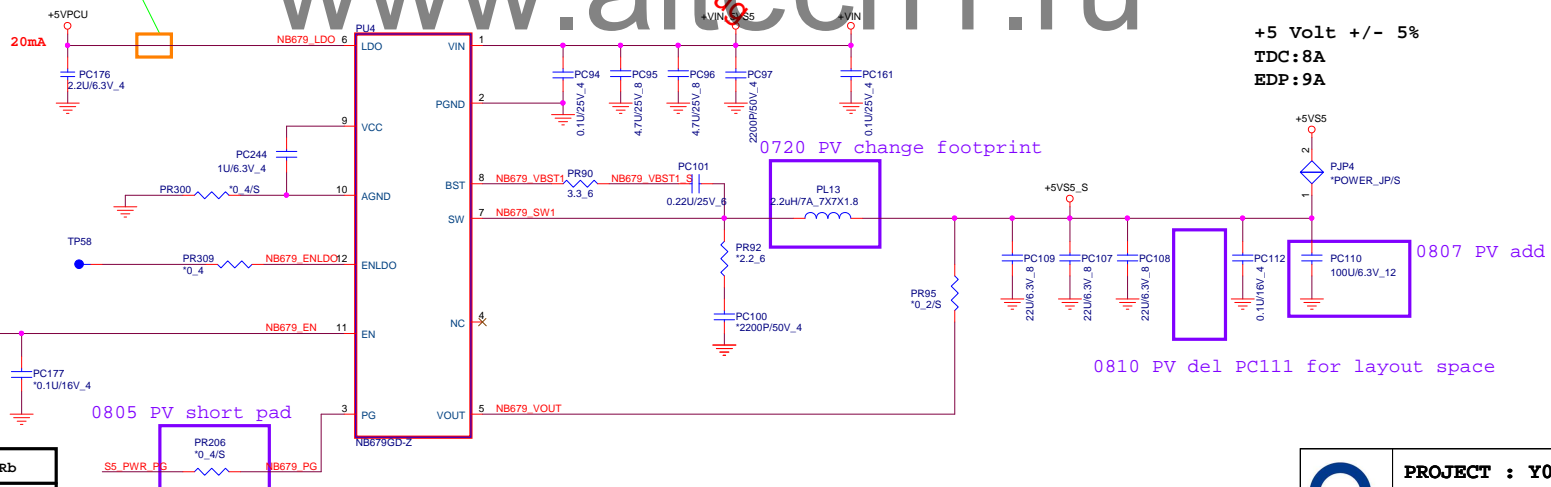
Do Not add test pad on VCC & LDO pin




+1.8VPCU Volt +/- 5%
Countinue current:0.01A
Peak current:0.02A



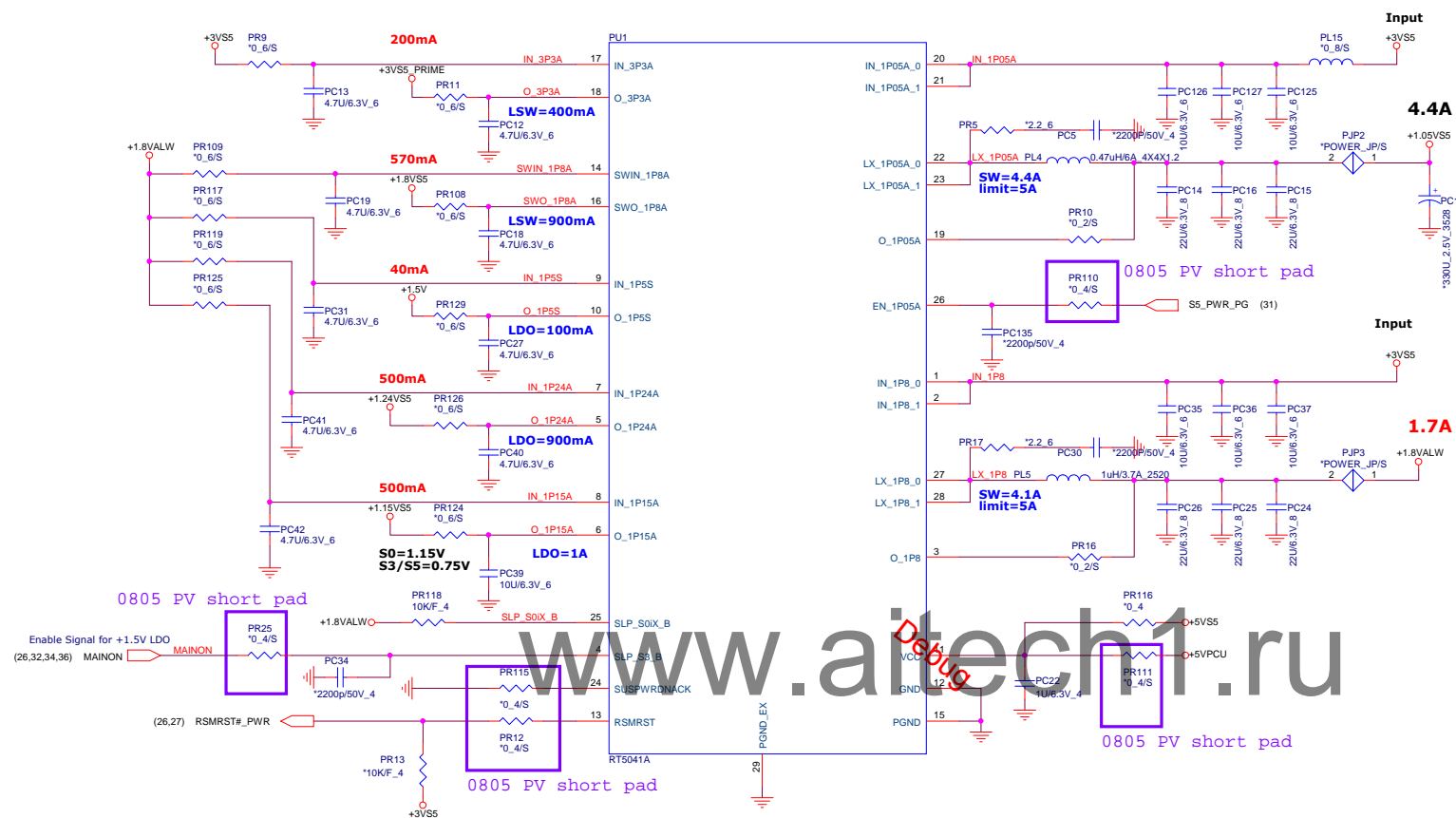
Do Not add test pad on VCC & LDO pin



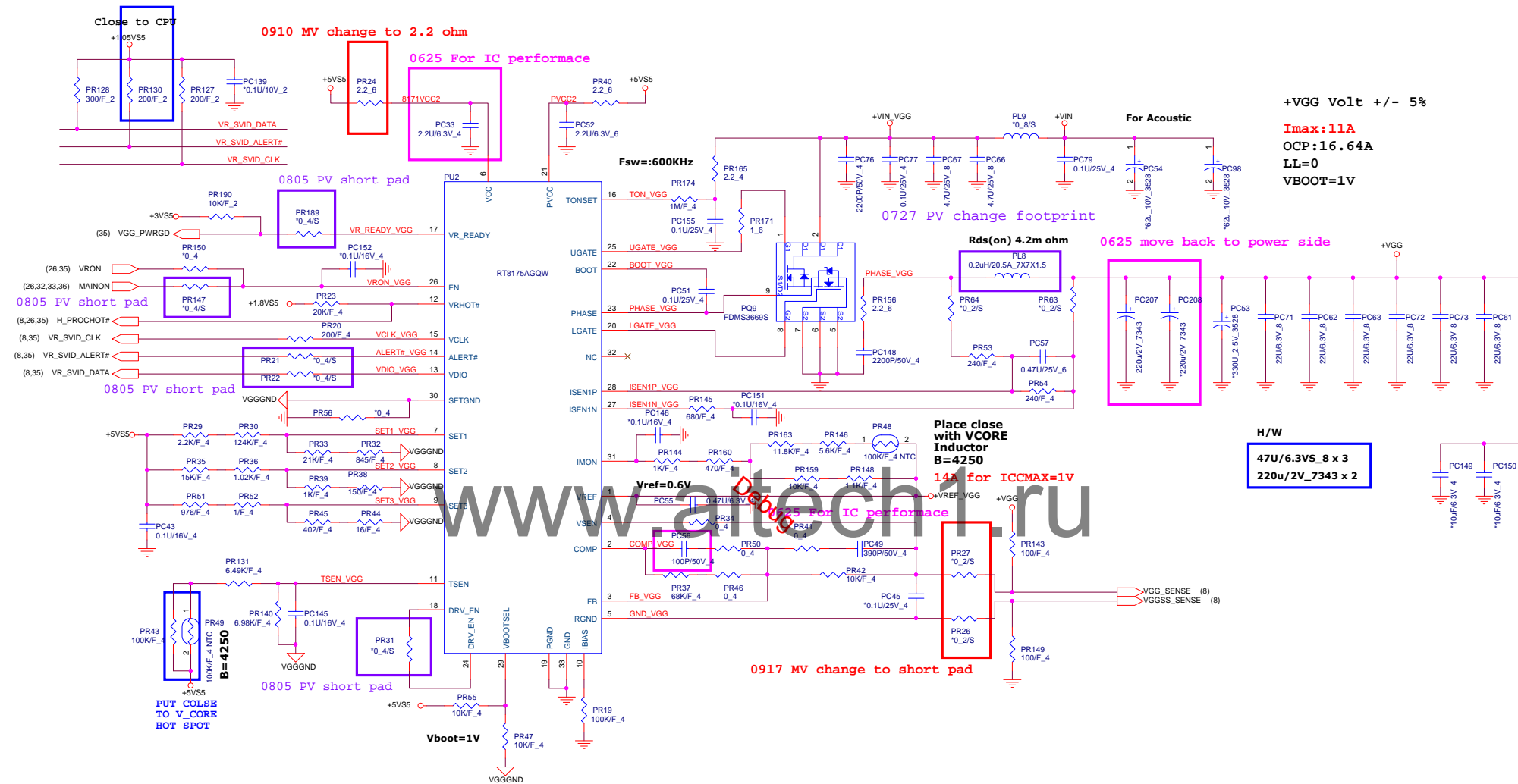
USB Charge support	Ra	Rb
Vine (No support)	Stuff	NA
Envy (Support)	NA	Stuff

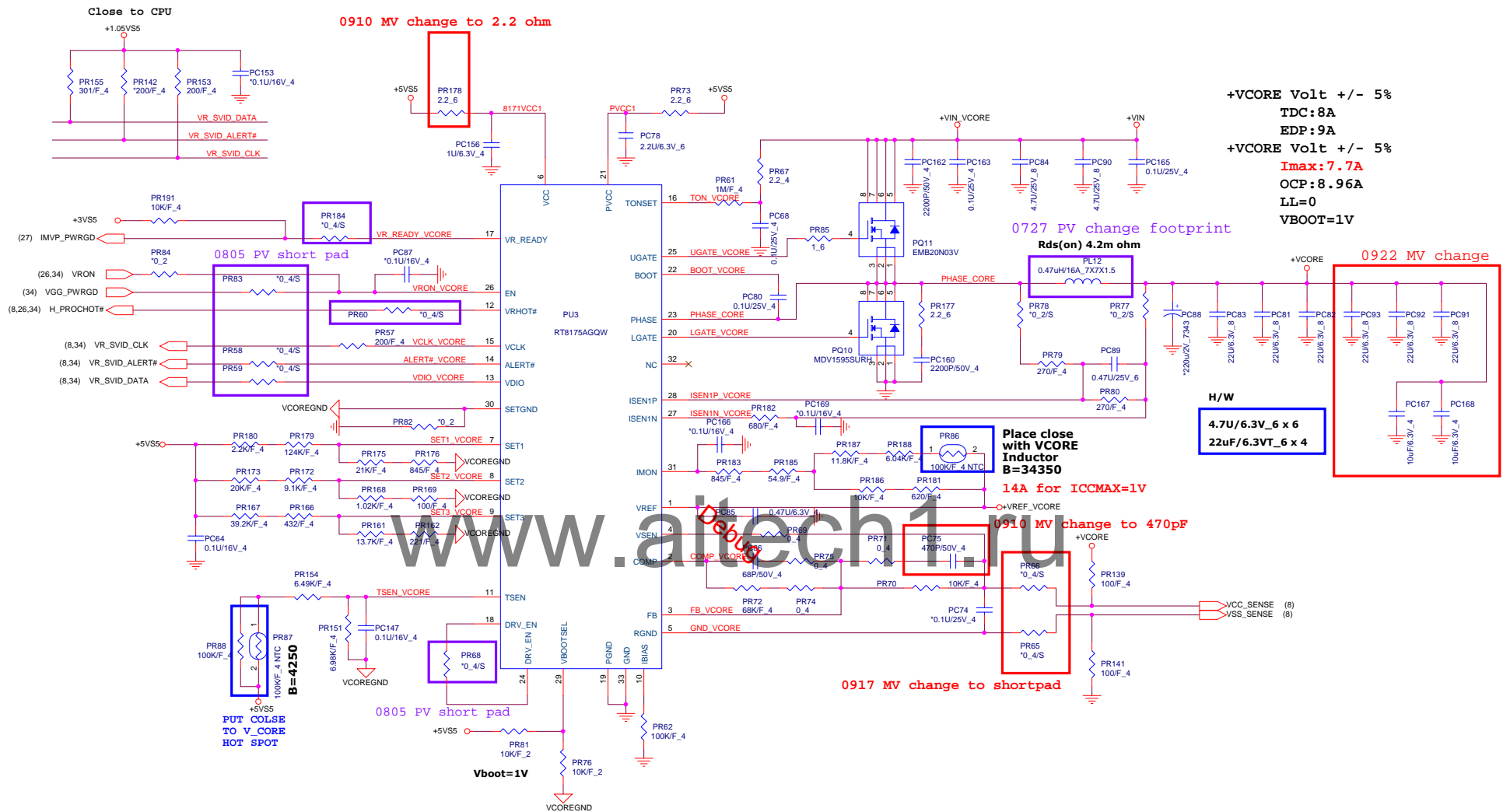
 NB5	PROJECT : Y0HB Quanta Computer Inc.		
	Size Custom	Document Number 3/5VPCU(SY8208B/SY8208C)	Rev 1A
	Date: Wednesday, September 23, 2013 Sheet 31 of 39		

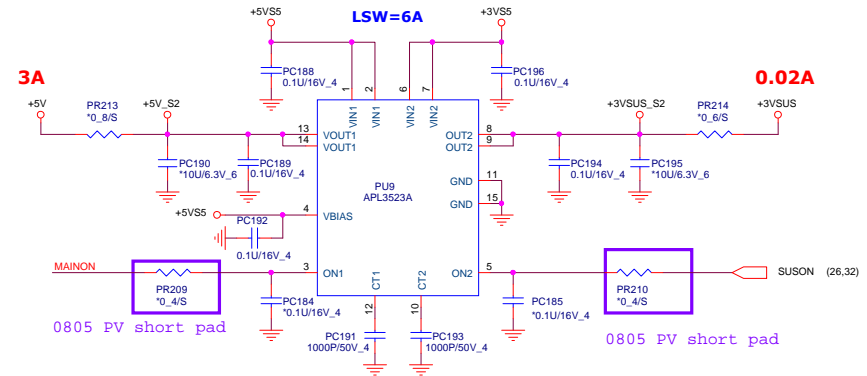
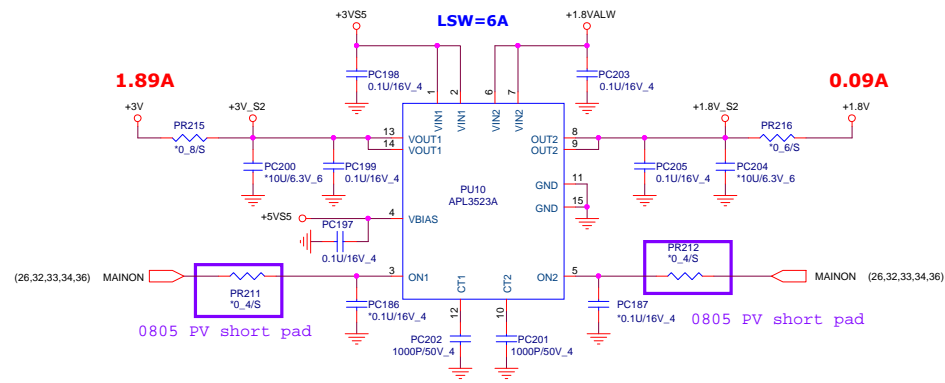




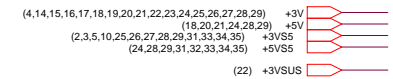
-
- +3VSS (2,3,5,10,25,26,27,28,29,31,34,35,36)
 +1.8VALW (36)
 +1.8VSS (4,5,6,7,8,10,12,16,18,23,26,27,34)
 +3VSS_PRIME (10,23,26)
 +1.5V (10,20)
 +1.24VSS (10)
 +1.15VSS (9,33)
 +5VPCU (31,33)
 +1.05VSS (8,9,34,35)
 +1.15VSS (9,33)
 +5VPCU (31,33)
 +1.8V (4,5,16,36)




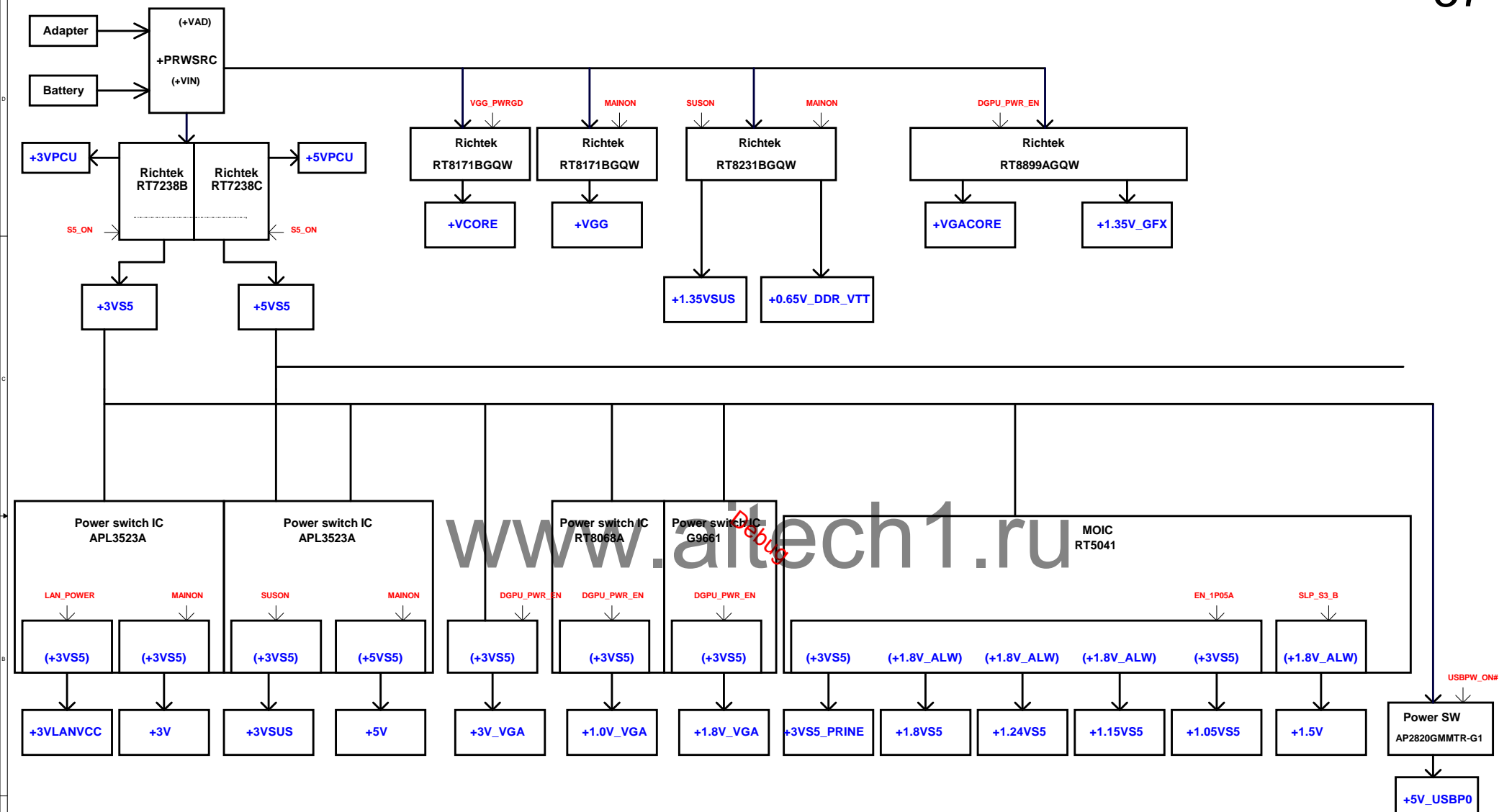


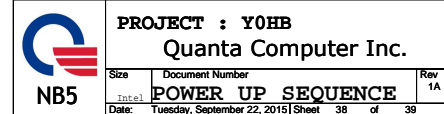


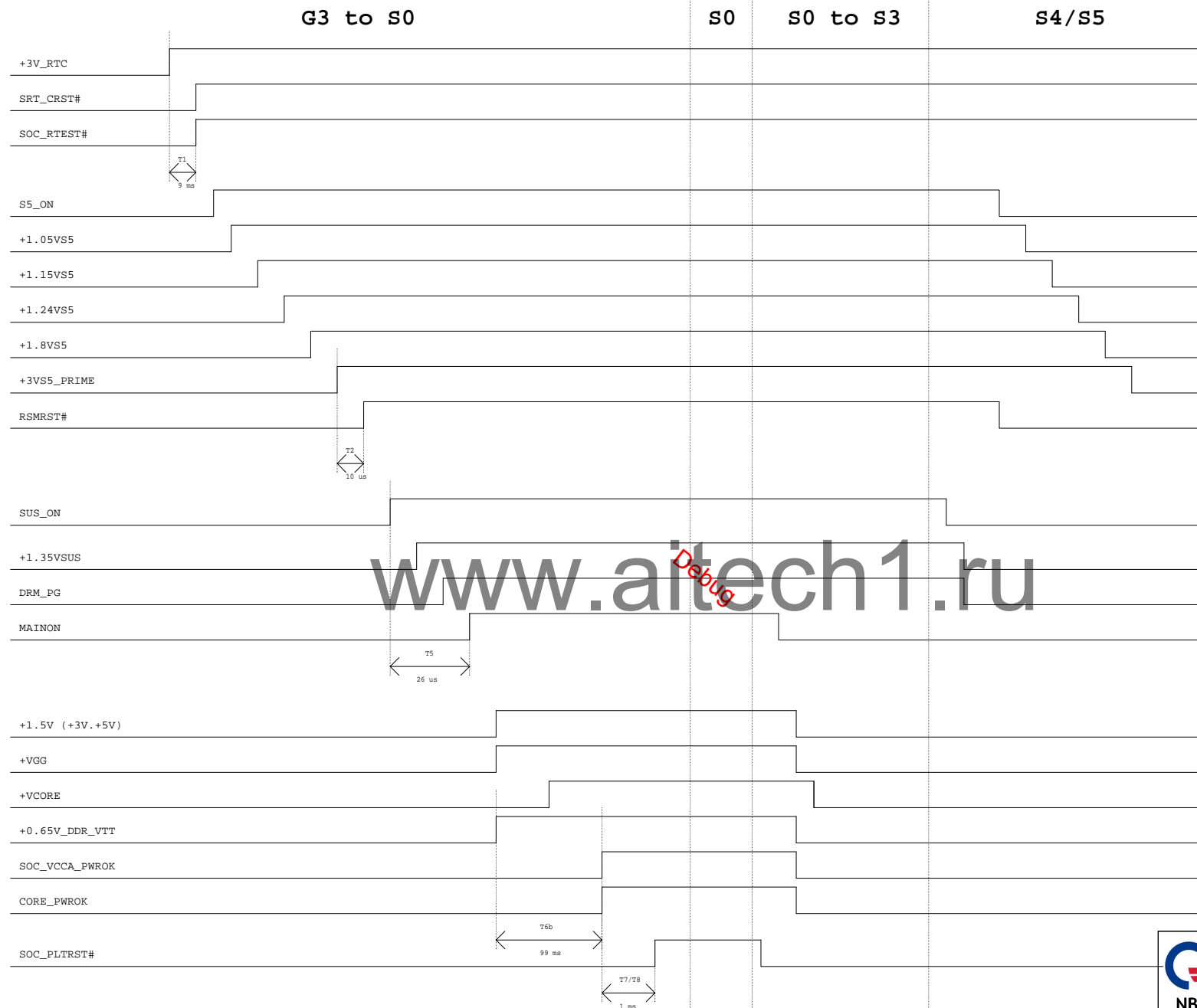
www.aitech1.ru



	PROJECT : Y0HB		
	Quanta Computer Inc.		
Size	Document Number	Rev	
NB5	Dis-charge IC (G5934RZ1U)	1A	
Date:	Wednesday, September 23, 2010	Sheet	36 of 39







PROJECT : Y0HB
Quanta Computer Inc.

Size: Document Number
Total: POWER UP SEQUENCE
Date: Tuesday, September 22, 2015 Sheet 39 of 39

Rev
1A